the commands and addresses from the command and address bus and driving the commands and

addresses to the plurality of memory devices, wherein the command buffer is shared by the

plurality of memory devices; and

      [c)]   a data buffer [register] connected between the plurality of memory devices

and the bidirectional data bus, the data buffer [register] receiving and latching the data

information from the bidirectional data bus and driving the data information to the plurality of

memory devices for a write operation, the data buffer [register] receiving and latching the data

information from the plurality of memory devices and driving the data information to the

bidirectional data bus for a read operation, wherein the data buffer is shared by the plurality of

memory devices.

6.   (Amended) The memory system according to claim 5, wherein the memory controller

communicates the commands and addresses and the data information using a pipelined packet-

protocol which incorporates a first delay introduced by the command buffer [register] of one of

the plurality of pipelined memory subsystems and a second delay introduced by the data buffer

[register] of one of the plurality of pipelined memory subsystems.

29.   (Amended) A method of retrieving data in a pipelined memory system, having a plurality

of memory subsystems, wherein each memory subsystem includes a command buffer [register], a

data buffer [register] and a plurality of memory devices, wherein each memory device includes

addressable storage, a data in and a data out buffer, a column decoder and a row decoder,

comprising:

      issuing commands and addresses on a unidirectional command and address bus;

      latching the commands and addresses in the command buffers [buffer registers];

      driving the latched commands and addresses to the column and row decoders;

      retrieving data from the addressable storage of one of the plurality of memory devices;

      latching the data in the data buffer of the one memory device [registers]; and

      receiving the data on a bidirectional data bus.

31.   (Amended) The method of retrieving data in a pipelined memory system according to claim 29 wherein issuing commands and addresses and receiving data communicates according to a packet protocol which incorporates a first delay introduced by the command buffer [register] and a second delay introduced by the data buffer [register].

32.   (Amended) A method of storing data in a pipelined memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a command buffer [register], a data buffer [register] and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising:

          issuing commands and addresses on a unidirectional command and address bus;

          issuing data on a bidirectional data bus;

          latching the commands and addresses in the plurality of command buffers [buffer registers];

          latching the data in the plurality of data buffers [registers];

          driving the latched commands and addresses to the column and row decoders;

          driving the latched data to the data in buffers; and

          storing the data in the addressable storage of the plurality of memory devices.

33.   (Amended) The method of claim 32, wherein issuing commands and addresses and issuing data include executing a packet protocol which incorporates a first delay introduced by the command buffer [register] of one of the plurality of memory subsystems and a second delay introduced by the data buffer [register] of one of the plurality of memory subsystems.

34.   (Amended) An electronic system comprising:

          a microprocessor;

          a memory controller coupled to the microprocessor;

          a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

          a bidirectional data bus coupled to the memory controller, the memory controller

communicating data information to the bidirectional data bus for a write operation and receiving

the data information from the bidirectional data bus during a read operation; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem

includes:

[a)]   a plurality M of memory devices wherein each memory device contains a

data in and a data out buffer, a column decoder and a row decoder;

[b)]   a command buffer [register] connected between the command and address

bus and the plurality of memory devices, the command buffer [register] receiving and

latching the commands and addresses from the command and address bus and driving the

commands and addresses to the plurality of memory devices, wherein the command

buffer is shared by the plurality of memory devices; and

[c)]   a data buffer [register] connected between the plurality of memory devices

and the bidirectional data bus, the data buffer [register] receiving and latching the data

information from the bidirectional data bus and driving the data information to the

plurality of memory devices for a write operation, the data buffer [register] receiving and

latching the data information from the plurality of memory devices and driving the data

information to the bidirectional data bus for a read operation.

35.   (Amended) The electronic system of claim 34, wherein the memory controller

communicates the commands and addresses and data information using a pipelined packet-

protocol which incorporates a first delay introduced by the command buffer [register] of one of

the plurality of pipelined memory subsystems and a second delay introduced by the data buffer

[register] of one of the plurality of pipelined memory subsystems.

38.   (Amended) A method of performing a memory transaction in an electronic system

having a memory controller and a plurality of memory subsystems, wherein each memory

subsystem includes a command buffer [register], a data buffer [register] and a plurality of

memory devices, wherein each memory device includes a data in and a data out buffer, a column

decoder and a row decoder, comprising:

issuing information to the memory controller;

issuing commands and addresses on a unidirectional command and address bus;

issuing data on a bidirectional data bus;

latching the commands and addresses received from the unidirectional command and address bus in the command buffers [buffer registers] of the plurality of memory subsystems;

driving the latched commands and addresses to the plurality of memory devices; and

if the memory transaction is a write, receiving and latching the data in the data buffers [registers] of the plurality of memory subsystems and driving the latched data to the plurality of memory devices.

39.   (Amended) The method of claim 38, wherein issuing commands and addresses and issuing data include executing a packet protocol which incorporates a first delay introduced by the command buffer [register] and a second delay introduced by the data buffer [register].

40.   (Amended) A method of storing data, in an electronic system, having a memory controller and a plurality of memory subsystems, wherein each memory subsystem includes a command buffer [register], a data buffer [register] and a plurality of memory devices, wherein each memory device includes a data in and a data out buffer, a column decoder and a row decoder, comprising:

issuing information to the memory controller, wherein the memory controller receives the information and wherein the memory controller issues commands and addresses on a unidirectional command and address bus;

issuing data on a bidirectional data bus;

latching the commands and addresses read from the unidirectional command and address bus in the command buffers [buffer registers] of the plurality of memory subsystems;

latching the data received from the bidirectional data bus in the data buffers [registers] of the plurality of memory subsystems;

driving the latched commands and addresses to the plurality of memory devices;

driving the latched data to the plurality of memory devices; and

storing the data in addressable storage of the plurality of memory devices.

41.   (Amended) The method of claim 40, wherein issuing commands and addresses and issuing data include executing a packet protocol which incorporates a first delay introduced by the command buffer [register] and a second delay introduced by the data buffer [register].

42.   (Amended) In an electronic system having a memory controller and a plurality of memory subsystems, wherein each memory subsystem includes a command buffer [register], a data buffer [register] and a plurality of memory devices, wherein each memory device includes a data in and a data out buffer, a column decoder and a row decoder, a method of retrieving data comprising:

    issuing information to the memory controller;

    issuing commands and addresses on a unidirectional command and address bus;

    latching the commands and addresses read from the unidirectional command and address bus in the command buffers [buffer registers] of the plurality of memory subsystems;

    driving the latched commands and addresses to the plurality of memory devices of the plurality of memory subsystems;

    retrieving data from addressable storage of the plurality of memory devices of the plurality of memory subsystems;

    latching the data in the data buffers [register] of the plurality of memory devices of the plurality of memory subsystems; and

    receiving the data on a bidirectional data bus.

43.   (Amended) The method of claim 42, wherein issuing commands and addresses and receiving data include executing a packet protocol which incorporates a first delay introduced by the command buffer [register] and a second delay introduced by the data buffer [register].

44.   (Amended) A memory system comprising:

    a unidirectional command and address bus coupleable to a memory control device;

    a bidirectional data bus coupleable to the memory control device; and

    a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

[a)]   a plurality M of memory devices wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder;

[b)]   a command buffer [register] connected between the command and address bus and the plurality of memory devices, the command buffer [register] receiving and latching commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices, wherein the command buffer is shared by the plurality of memory devices; and

[c)]   a data buffer [register] connected between the plurality of memory devices and the bidirectional data bus, the data buffer [register] receiving and latching data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data buffer [register] receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

45.   (Amended) The memory system of claim 44, wherein the commands and addresses and the data information communicate using a pipelined packet-protocol which incorporates a first delay introduced by the command buffer register of one of the plurality of pipelined memory subsystems and a second delay introduced by the data buffer [register] of one of the plurality of pipelined memory subsystems.

48.   (Amended) A method of storing data in a pipeline memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a command buffer [register], a data buffer [register] and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising:

          receiving commands and addresses from a unidirectional command and address bus;

          receiving data from a bidirectional data bus;

          latching the commands and addresses in the plurality of command buffers [buffer registers];

          latching the data in the plurality of data buffers [registers];

driving the latched commands and addresses to the column and row decoders;

driving the latched data to the data in buffers; and

storing the data in the addressable storage of the plurality of memory devices.

49.   (Amended) The method of claim 48, wherein receiving commands and addresses and receiving data include executing a packet protocol which incorporates a first delay introduced by the command buffer [register] and a second delay introduced by the data buffer [register].

50.   (Amended) A method of retrieving data in a pipeline memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a command buffer [register], a data buffer [register] and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising:

        receiving commands and addresses from a unidirectional command and address bus;

        latching the commands and addresses in the plurality of command buffers [buffer registers];

        driving the latched commands and addresses to the column and row decoders;

        retrieving data from the addressable storage of the plurality of memory devices;

        latching the data in the plurality of data buffers [registers]; and

        driving the data onto a data bus.

51.   (Amended) The method of claim 50, wherein receiving commands and addresses and driving the data include executing a packet protocol which incorporates a first delay introduced by the command buffer [register] and a second delay introduced by the data buffer [register].

52.   (Amended) A memory system, comprising:

        a unidirectional command and address bus in electrical communication with a memory control device;

        a bidirectional data bus in electrical communication with the memory control device; and

        a plurality N of pipelined memory subsystems, wherein each memory subsystem

includes:

[a)]   a plurality M of memory devices wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder;

[b)]   a command buffer [register] connected between the command and address bus and the plurality of memory devices, the command buffer [register] receiving and latching commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices, wherein the command buffer is shared by the plurality of memory devices; and

[c)]   a data buffer [register] connected between the plurality of memory devices and the bidirectional data bus, the data buffer [register] receiving and latching data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data buffer [register] receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

53.   (Amended) The memory system of claim 52, wherein the commands and addresses and the data information communicate using a pipelined packet-protocol which incorporates a first delay introduced by the command buffer [register] of one of the plurality of pipelined memory subsystems and a second delay introduced by the data buffer [register] of one of the plurality of pipelined memory subsystems.

56.   (Amended) A method of retrieving data in a pipelined memory system, comprising:

issuing commands and addresses on a unidirectional command and address bus to a plurality of memory subsystems;

latching the commands and addresses in a command buffer [register] in each of the plurality of memory subsystems;

driving the latched commands and addresses to column and row decoders in each of the plurality of subsystems;

retrieving data from addressable storage of one of the plurality of memory subsystems;

latching the data in a data buffer [register] of the one of the plurality of memory

subsystems; and

receiving the data on a bidirectional data bus.

Please add the following new claims:

57.   (New) A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a plurality M of memory devices wherein each memory device consists of a data in and a data out buffer, a decoder and an array of memory cells;

a command buffer connected between the command and address bus and the plurality of memory devices, the command buffer receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices, wherein the command buffer is shared by the plurality of memory devices; and

a data buffer connected between the plurality of memory devices and the bidirectional data bus, the data buffer receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data buffer receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

58.   (New) The memory system of claim 57, wherein the data buffer is shared by the plurality of memory devices.

59.   (New) The memory system of claim 5, wherein N equals eight.

60.   (New) The memory system of claim 5, wherein M equals eight.

61.   (New) The memory system of claim 5, wherein each of the memory devices includes an
addressable storage.

62.   (New) The system according to claim 5, wherein the bidirectional data bus is a single 16
bit bus, supports 64 data buffers, and operates at 800 MHz.

63.   (New) A method of operating the memory system of claim 5, comprising:
        issuing commands and addresses on the unidirectional command and address bus;
        latching the commands and addresses in the command buffers;
        driving the latched commands and addresses to the column and row decoders;
        retrieving data from addressable storage of one of the plurality of memory devices;
        latching the data in the data buffers; and
        receiving the data on the bidirectional data bus.

64.   (New) The electronic system of claim 34, wherein the data buffer is shared by the
plurality of memory devices.

65.   (New) The memory system of claim 44, wherein the data buffer is shared by the plurality
of memory devices.

66.   (New) The memory system of claim 52, wherein the data buffer is shared by the plurality
of memory devices.

67.   (New) A memory system comprising:
        a memory controller;
        a unidirectional command and address bus coupled to the memory controller, the memory

controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

plurality M of memory devices wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder;

a command buffer connected between the command and address bus and the plurality of memory devices, the command buffer receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a data buffer connected between the plurality of memory devices and the bidirectional data bus, the data buffer receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data buffer receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation, wherein the data buffer is shared by the plurality of memory devices.

68.   (New) The memory system according to claim 67, wherein the memory controller communicates the commands and addresses and the data information using a pipelined packet-protocol which incorporates a first delay introduced by the command buffer of one of the plurality of pipelined memory subsystems and a second delay introduced by the data buffer of one of the plurality of pipelined memory subsystems.

69.   (New) The memory system according to claim 67, wherein each memory device is a dynamic random access memory device.

70.   (New) The memory system according to claim 67, wherein each of the plurality N of pipelined memory subsystems includes eight memory devices and wherein N equals eight.